## REMARKS

The above amendments and following remarks are submitted in response to the Official Action of the Examiner mailed December 8, 2003. Having addressed all objections and grounds of rejection, claims 1-25, being all the pending claims, are now deemed in condition for allowance. Reconsideration to that end is respectfully requested.

The Examiner has rejected claims 11 and 16 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,397,300, issued to Arimilli et al (hereinafter referred to as "Arimilli"). Claims 11 and 16 have been herewith amended. The rejection of claims 11 and 16, as amended, is respectfully traversed for the following reasons.

Regarding amended method claim 11, step b requires a "hit" in the level one cache memory rather than a "miss". Support for this position may be found in Fig. 4, element 90, and in the specification at page 15, lines 5-9. Claim 11, as amended, is readily distinguishable from Arimilli. The claimed invention requires a level one cache memory hit followed by a level two cache memory hit before the invalidation of the corresponding level one cache memory element. Arimilli, on the other hand, invalidates the level one cache line without regard to whether there is a level two cache memory hit (see column 12, lines 22-25). This distinction is rather substantial if one considers a

write request with a level one cache memory hit without a level two cache memory hit. Because Arimilli would invalidate the level one cache line, it must await sequential level three write and read accesses before the affected cache line can again be accessed. Applicants' invention is more efficient in that it relies upon the level two cache memory during whatever time may be required to update the level three memory.

Therefore, the rejection of claim 11, as amended, along with all claims depending therefrom, is respectfully traversed.

Claim 16 has also been rejected as anticipated by Arimilli. Claim 16 has been amended for certain editorial concerns. However, it has also been amended to provide invalidation of a level one cache memory data element if there is both level one and level two cache memories hits. Thus, claim 16, as amended, becomes patentable for the reasons discussed above with regard to claim 11. The rejection of claim 16, and all claims depending therefrom, is respectfully traversed.

Claims 1-3 have been rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,253,291, issued to Pong et al (hereinafter referred to as "Pong") in view of U.S. Patent No. 6,061,766, issued to Lynch et al (hereinafter referred to as "Lynch"). In response thereto, claim 1 has been amended to remove the provision of invalidation if there is a write ownership request. Though Applicants had intended that the

"first logic" be read as "inclusive Or" with regard to the invalidate conditions, apparently, the Examiner has read the invalidation conditions of the "first logic" as an exclusive "or". He states:

> processor invalidate data in their own memories (or on-chip caches) when request for exclusive use if granted; col. 1, lines 40-48, 53-55;

Therefore, having removed the "write ownership request" as an invalidate condition, removes the ambiguity and ensures the alleged combination does not meet the claim limitations.

As a result, the rejection of claims 1-3, as amended, is respectfully traversed.

In rejecting claim 2, the Examiner states:

> ....the use of multiple logics is an inherent feature of any computer system.

Though this tends to be a reasonable inference, it does not comply with MPEP 2112 which specifically requires that inherency can be found only when the condition exists "of necessity". The Examiner has made no such showing. Furthermore, even if he had complied with MPEP 2112, claim 2 requires multiple logics which perform specific functions. Not only is this not "inherent" as a matter of law, it is not "inherent" as a matter of fact. The rejection of claim 2 is respectfully traversed.

The Examiner repeats the same finding with regard to his rejection of claim 3. Therefore, the rejection of claim 3 is respectfully traversed for the same reason.

Claim 4 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Pong in view of Lynch and further in view of U.S. Patent No. 6,425,060, issued to Mounes-Toussi et al (hereinafter referred to as "Mounes-Toussi"). In response thereto, claim 4 has been amended to indicate that it is limited to the location of the requested data which is recorded rather than the requested data itself. This feature is not shown in the alleged combination. Therefore, the rejection of claim 4, as amended, is respectfully traversed.

Claim 5 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Pong in view of Lynch and further in view of U.S. Patent No. 4,891,809, issued to Hazawa (hereinafter referred to as "Hazawa"). This ground of rejection is respectfully traversed. Claims 5 depends from claim 1 and is further limited by a "fifth logic" which invalidates a data entity in the level one cache memory in response to the finding of a parity error in a corresponding data entity of the level two cache memory. Hazawa shows only one cache memory unit (i.e., cache memory unit 2). Pong and Lynch show no parity checking facilities. Therefore, the alleged combination does not have the elements of the claimed invention. The rejection of claim 5 is respectfully traversed.

Claim 6 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Pong in view of Arimilli et al. In response

thereto, claim 6 has been amended to provide invalidation upon the coincidence of both level one cache memory write hit and level two cache memory hit. This is not present in the alleged combination.

Furthermore, the alleged combination would render the claimed improvement of Pong inoperative, because it requires strict FIFO for all first category accesses, which would not accommodate the invalidation of the level one cache memory data element. The rejection of claim 6, as amended, and all claims depending therefrom, is respectfully traversed.

Claims 7-8 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Pong in view of Arimilli and further in view of Lynch. In making his rejection, the Examiner states:

> ....snoop requests checks for the presence of an object in cache; only requests for exclusive use which match cache tags are invalidated...

Claim 7 depends from claim 6 and contains all of the limitations thereof. As a result, the invalidation involves only local ownership. The snoop request of Lynch involves only remote ownership. The rejection of claim 7 is respectfully traversed.

In invalidating claim 8, the Examiner states:

> It is clearly obvious that any computer system uses a combination of logic to produce output based on the rules of logic it is designed to follow; clearly, the use of multiple logics is an inherent feature of any computer system.

This statement indicates that the Examiner's findings are both clearly erroneous and not consistent with controlling law. The issue presented by MPEP 2112 is not whether a hypothetical computer has multiple logics, it is whether the alleged combination has the claimed logic structure in performance of the claimed functionality. Not only has the Examiner not met his burden of proof under MPEP 2112, he has not even attempted to do so, because he cannot. The rejection of claim 8 is respectfully traversed.

Claim 9 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Pong in view of Arimilli and further in view of Mounes-Toussi. As with claim 5, claim 9 has been herewith amended and is now deemed to distinguish from the alleged combination because claim 9 is now limited to recording of the location rather than the requested data. The rejection of claim 9 is respectfully traversed.

Claim 10 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Pong in view of Arimilli and further in view of Hazawa. As indicated above, Hazawa has a single cache memory unit 2. Neither Pong nor Arimilli has a parity checking facility. It is deemed clearly erroneous to find that the alleged combination could teach invalidating of a level one cache memory data element in response to detection of a parity error in

a level two cache memory data element. The rejection of claim 10 is respectfully traversed.

Claims 12-13 and 17-18 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of Lynch. As to claims 12 and 17, the ownership is local ownership. The snoop provides information regarding remote ownership. The rejection of claims 12 and 17 is respectfully traversed.

In rejecting claims 13 and 18, the Examiner again apparently attempts to find inherency without complying with his burden under MPEP 2112. The rejection of claims 13 and 18 is respectfully traversed.

Claims 14 and 19 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of Mounes-Toussi. In response thereto, claims 14 and 19 have been amended to clearly require recording of the location of the data element rather than the data element. The rejection of claims 14 and 19 is respectfully traversed.

Claims 15 and 20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of Hazawa. As explained above, Hazawa has a single cache memory unit 2. It certainly does not teach invalidation of a data element in one cache memory unit in response to a parity error in a different cache memory unit. The rejection of claims 15 and 20 is respectfully traversed.

Newly presented claims 21-25 are deemed independently patentable in view of the arguments presented above.

Having thus responded to each objection and ground of rejection, Applicants respectfully request entry of this amendment and allowance of claims 1-25, being the only pending claims.

Respectfully submitted,

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By his attorney,

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